REMARKS

The continued allowance of claims 2-11 and 17, and conditional allowance of claims 18-21 and 27 is noted, with thanks.

Claims 3, 4, 7, 8, 18, 19, 21, 31 have been amended to correct minor informalities and to clarify the invention.

No new matter has been entered by any of the foregoing amendments.

Turning to the Examiner's objections as to the claims, the objection as to "said drain" in line 37 of claim 19 is believed to be in error. The remainder of the objections have been addressed as suggested by the Examiner. Thus, it is believed all of the Examiner's objections have been overcome.

Turning to the rejection of claim 31 under 35 USC §112 as indefinite, claim 31 has been amended to clarify that a cathode grounded diode is a separate element in the claim. Thus, it is believed the Examiner's §112 rejection has been overcome.

Turning to the rejection of claims 28 and 29 under 35 USC §102 as anticipated by McNeill et al. (U.S. Patent No. 6,150,872), and the rejection of claims 30 and 31 as obvious from McNeill et al., the Examiner's rejections are in error. McNeill et al. discloses an operational amplifier, but never discloses an operational transconductance amplifier. As the Examiner is aware, an operational amplifier is a device that directly compares two voltage levels or voltage signals and it provides an amplified output voltage signal response based at least in part on the voltage signal comparison. However, an OTA receives a differential input voltage and outputs a current. This difference can be seen more clearly by comparing FIG. 1 of McNeill et al. to FIG. 1 of the instant invention.

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In FIG. 1 of McNeill et al., VAMP1 equalizes the voltages at nodes N1 and N2. The voltage at 106 (emitter of Q1) is different from the voltage at 108 (emitter of Q2), which will become equal due to a voltage drop at R1 (110) resulting in a voltage of V(N1)-V(N2) at VAMP1. However, in FIG. 1 of the present invention, a resistor which would correspond to R1 of McNeill et al. is missing.

In addition, FIG. 1 of McNeill et al., depicts a current (20 μA) flowing across M3 that is current-mirror-reflected by the current-mirror circuit 170, and output voltage VBT that is obtained by adding a corresponding voltage drop (R2 * 20 μA) at resistor R2 to V(N2). However, in Applicant's invention, different voltages VBE1 and VBE2 obtained from Q1 and Q2, respectively, are supplied to OTA1, which outputs a current (gm1 * Δ VBE) that is proportional to the difference between the differential voltages (Δ VBE=VBE2 - VBE1). The current output from OTA1 is amplified by a factor of K2 by a current mirror circuit 13 and supplied to one input terminal (+) of OTA2. This input terminal (+) of OTA2 is also connected to the output terminal of OTA2, while the other input terminal of OTA2 is connected to voltage VBE2 output from Q2. The reference voltage VREF is obtained because OTA2 ensures that a current (gm2 * (VREF-VBE2)) proportional with a difference (VREF-VBE2) between the output voltage VREF of OTA2 and a voltage VBE2 output from Q2 will become equal to a current (K2 * gm 1 * ΔVBE) from the current mirror 13. Thus, the resistors (R1, R2) for conversion into voltage are essential for the circuit of McNeill et al., whereas such resistors are unnecessary in the present invention.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

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Respectfully submitted,

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